

Integrated Circuit Design 4th Edition

Weste Solution

Timing closure ; Harris, David Money (2011). "VLSI Design Flow";. (2014-11-14). SlideServe. Weste, Neil H. Retrieved 2025-06-18. E. The goal is to guarantee correct data transfer and reliable operation at the target clock frequency. CMOS VLSI design: a circuits and systems perspective Timing closure in VLSI design and electronics engineering is the iterative design process of assuring all electromagnetic signals satisfy the timing requirements of logic gates in a clocked synchronous circuit, such as timing constraints, clock period, relative to the system clock 328237f6df

A synchronous circuit is composed of two types of primitive elements: combinatorial logic gates (NOT, AND, OR, NAND, NOR, XOR etc.), which process logic functions without memory, and sequential elements (flip-flops, latches, registers), which can store data and are triggered by clock signals. Through timing closure, the circuit can be adjusted through layout improvement and netlist restructuring to reduce path delays... 328237f6df

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